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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,724	02/10/2004	Masatoshi Yasutake	S004-5210	3824

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ADAMS & WILKS
17 BATTERY PLACE
SUITE 1231
NEW YORK, NY 10004

EXAMINER	
JEFFERSON, QUOVAUNDA	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 06/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,724	YASUTAKE ET AL.	
	Examiner	Art Unit	
	Quovaunda Jefferson	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 36-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 36-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 36, 37, 47 and 48 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirose, US Patent 6,826,971 (herein referred to as Hirose'971).

Regarding claim 1, Hirose'971 teaches a method of preparing a sample chip and observing a wall surface thereof, comprising the steps of a first step of etching a preselected portion of a sample and an area surrounding the preselected portion of by irradiating the sample with a focused ion beam to form a sample chip having a wall surface with stepped potions formed (the preselected area is the area of the defect **3** and an area surrounding the preselected portion would be everything else on chip **2** and the chip has several wall surfaces formed. See column 4, lines 46 to column 5, line 17), a second step of taking out the sample chip from the sample (column 5, line 18-23), and

a third step of observing a the wall surface of the taken sample chip with a scanning probe microscope (SPM) (column 7, line 55).

Regarding claim 36, Hirose '971 teaches a method of preparing a sample chip and observing a wall surface thereof, comprising the steps of a first step of etching a preselected portion of a sample and an area surrounding the preselected portion of the sample by irradiating the sample with a first focused energy beam to form a sample chip (the preselected area is the area of the defect **3** and an area surrounding the preselected portion would be everything else on chip **2** and the chip has several wall surfaces formed. See column 4, lines 46 to column 5, line 17), a second step of picking-up the sample chip from the sample (column 5, line 18-23), a third step of irradiating a wall surface of the sample chip with a second focused energy beam to thereby etch the wall surface (when the microprober is taken off the surface of the chip in column 5, lines 18-23 and where the defect **3** in column 5, lines 57-61), and a fourth step of observing the etched wall surface of the sample chip using a scanning probe microscope (column 7, line 55).

Regarding claim 37, Hirose'971 further teaches the second step further comprises the step of securing the sample chip to a sample chip holder **25** after the sample chip is picked-up from the sample (with microprobers **22)** so that the wall surface of the sample chip etched in the third step (column 5, lines 57-61) and observed in the fourth step faces in an upward direction (In figure 10, the defect can be viewed

from 53a in a TEM or SEM microscope, showing a view as shown in figure 11 as defect 3)

Regarding claim 47, Hirose'971 teaches a method of preparing a sample chip and observing a wall surface thereof, comprising the steps of providing a sample having a multi-layered structure made of different materials (column 1, lines 51-55), irradiating the sample with a focused energy beam to form a sample chip while a wall surface of the sample chip is gas-assist-etched so that the wall surface is formed with stepped portions due to differences in the materials of the multi-layered structure of the sample (see column 3, lines 60-67 and column 4, lines 1-17 where tungsten film, the stepped portion of the sample chip, is installed on the chip using tungsten gas when the gas is used with the focus ion beam), taking out the sample chip from the sample (column 5, lines 18-23), and observing the wall surface of the sample chip having the stepped portions with a scanning probe microscope (column 7, line 55).

Regarding claim 48, Hirose'971 further teaches the focused energy beam is a focused ion beam.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirose'971 as applied to claim 36 above, and further in view of Mizumura, US Patent 5,825,035.

Regarding claim 38, Hirose'971 further teaches the first focused energy beam is a focused ion beam (column 4, line 50), but fails to teach the second focused energy beam is an argon ion beam. Mizumura teaches a focus energy beam using an argon beam with the advantage of the ion beam can be irradiated onto a sample such as a silicon wafer without causing contamination of the sample with heavy metals (column 9, lines 26-35), which can then be used as a second focus energy beam in Hirose'971.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Mizumura with that of Hirose'971 because the focus ion beam using argon has with the advantage of the ion beam can be irradiated onto a sample such as a silicon wafer without causing contamination of the sample with heavy metals

Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirose'971 and Mizumura as applied to claim 38 above, and further in view of Hirose et al, US Patent 5,783,830 (herein referred to as Hirose'830).

Regarding claim 39, Hirose'971 fails to teach the first step includes the step of processing the sample chip to form stepped portions in the wall surface of the sample chip (rather, Hirose '971 teaches forming stepped portions **on** the wall surface of the chip). Hirose '830 teaches the first step includes the step of processing the sample chip to form stepped portions in the wall surface of the sample chip as a shape of sample that is first processed with the use of the focus ion beam (the sample having stepped portions from top to bottom and bottom to top. See figure 5A and column 3, lines 55-62).

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Hirose'830 with that of Hirose '971 as the shape of the sample that is first processed, which is to be used later for sample analysis (column 3, lines 55-62 and figure 5A)

Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirose, US Patent 6,826,971 (herein referred to as Hirose'971).

Regarding claim 40, Hirose'971 teaches a method of preparing a sample chip and observing a wall surface thereof, comprising the steps of a first step of etching a preselected portion of a sample and an area surrounding the preselected portion of the sample by irradiating the sample with a first focused energy beam to form a sample chip (the preselected area is the area of the defect **3** and an area surrounding the preselected portion would be everything else on chip **2** and the chip has several wall surfaces formed. See column 4, lines 46 to column 5, line 17), a second step of taking out the sample chip from the sample (column 5, line 18-23), a third step of irradiating a wall surface of the sample chip with a second focused energy beam thereby to etch the wall surface (when the microprober is taken off the surface of the chip in column 5, lines 18-23 and where the defect **3** in column 5, lines 57-61), a fourth step of observing the etched wall surface of the sample chip using a scanning probe microscope (column 7, line 55), and a fifth step of irradiating the observed wall surface of the sample chip with the first focused energy beam to thereby to etch the observed wall surface (to further explain, Hirose'971 teaches one method of observing the sample is through a TEM type of microscope. Hirose'971 explains that if necessary, the sample can be thinned using the focus ion beam. Therefore, one of ordinary skill in the art would know that after a first observation using a TEM or SPM, if the sample is too thick to observe, the sample would need to be thinned, using a FIB and that the sample can be thinned by irradiating the observed wall surface and/or any wall surface that is deemed necessary, then observing the sample again using a TEM or SPM), and a step of repeating the third to

fifth steps a preselected number of times (which can be done by repeat observing and irradiating to thin down the sample).

Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirose'971 as applied to claim 40 above, and further in view of Mizumura.

Regarding claim 41, Hirose'971 further teaches the first focused energy beam is a focused ion beam (column 4, line 50), but fails to teach the second focused energy beam is an argon ion beam. Mizumura teaches a focus energy beam using an argon beam with the advantage of the ion beam can be irradiated onto a sample such as a silicon wafer without causing contamination of the sample with heavy metals (column 9, lines 26-35), which can then be used as a second focus energy beam in Hirose'971.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Mizumura with that of Hirose'971because the focus ion beam using argon has with the advantage of the ion beam can be irradiated onto a sample such as a silicon wafer without causing contamination of the sample with heavy metals

Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirose '971 and Mizumura as applied to claim 41 above, and further in view of Hirose et al, US Patent 5,783,830 (herein referred to as Hirose'830).

Regarding claim 42, Hirose'971 fails to teach the first step includes the step of processing the sample chip to form stepped portions in the wall surface of the sample chip (rather, Hirose'971 teaches forming stepped portions **on** the wall surface of the chip). Hirose'830 teaches the first step includes the step of processing the sample chip to form stepped portions in the wall surface of the sample chip as a shape of sample that is first processed with the use of the focus ion beam (the sample having stepped portions from top to bottom and bottom to top. See figure 5A and column 3, lines 55-62).

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Hirose'830 with that of Hirose'971 as the shape of the sample that is first processed, which is to be used later for sample analysis (column 3, lines 55-62 and figure 5A)

Claims 43 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirose, US Patent 6,826,971 (herein referred to as Hirose'971).

Regarding claim 43, Hirose'971 teaches method of preparing a sample chip and observing a wall surface thereof, comprising the steps of a first step of etching a preselected portion of a sample and an area surrounding the preselected portion of the sample by irradiating the sample with a first focused energy beam to form a sample chip (the preselected area is the area of the defect **3** and an area surrounding the

preselected portion would be everything else on chip **2** and the chip has several wall surfaces formed. See column 4, lines 46 to column 5, line 17), a second step of taking out the sample chip from the sample (column 5, lines 18-23), a third step of irradiating a wall surface of the sample chip with a second focused energy beam thereby to etch the wall surface (when the microprober is taken off the surface of the chip in column 5, lines 18-23 and where the defect **3** in column 5, lines 57-61), a fourth step of observing the etched wall surface of the sample chip using a scanning probe microscope (column 7, line 55), a fifth step of irradiating the observed wall surface of the sample chip with the first focused energy beam to thereby to etch the observed wall surface(to further explain, Hirose'971 teaches one method of observing the sample is through a TEM type of microscope. Hirose'971 explains that if necessary, the sample can be thinned using the focus ion beam. Therefore, one of ordinary skill in the art would know that after a first observation using a TEM or SPM, if the sample is too thick to observe, the sample would need to be thinned, using a FIB and that the sample can be thinned by irradiating the observed wall surface and/or any wall surface that is deemed necessary, then observing the sample again using a TEM or SPM) and a step of repeating the fourth and fifth steps a reselected number of times (which can be done by repeat observing and irradiating to thin down the sample).

Regarding claim 46, Hirose further teaches comprising the step of forming the sample chip with a rectangular parallelepiped shape in an asymmetric form to facilitate identification of the wall surface of the sample chip in the fourth step. Notwithstanding, it

would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirose'971 as applied to claim 43 above, and further in view of Mizumura.

Regarding claim 44, Hirose'971 further teaches the first focused energy beam is a focused ion beam (column 4, line 50), but fails to teach the second focused energy beam is an argon ion beam. Mizumura teaches a focus energy beam using an argon beam with the advantage of the ion beam can irradiated onto a sample such as a silicon

wafer without causing contamination of the sample with heavy metals (column 9, lines 26-35), which can then be used as a second focus energy beam in Hirose'971.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Mizumura with that of because the focus ion beam using argon has with the advantage of the ion beam can be irradiated onto a sample such as a silicon wafer without causing contamination of the sample with heavy metals

Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirose '971 and Mizumura as applied to claim 44 above, and further in view of Hirose et al, US Patent 5,783,830 (herein referred to as Hirose'830).

Regarding claim 45, Hirose'971 fails to teach the first step includes the step of processing the sample chip to form stepped portions in the wall surface of the sample chip (rather, Hirose'971 teaches forming stepped portions **on** the wall surface of the chip). Hirose'830 teaches the first step includes the step of processing the sample chip to form stepped portions in the wall surface of the sample chip as a shape of sample that is first processed with the use of the focus ion beam (the sample having stepped portions from top to bottom and bottom to top. See figure 5A and column 3, lines 55-62).

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Hirose'830 with that of Hirose'971 as the shape of the sample that is first processed, which is to be used later for sample analysis (column 3, lines 55-62 and figure 5A).

Response to Amendment and Arguments

Applicant has amended claim 1, cancelled claims 2 and 3, and added new claims 36-48. Claims 1 and 36-48 are pending in this application.

Applicant argues on page 14 that Hirose '971 does not disclose or describe newly amended claim 1 amended limitation of "the formation of the sample chip with a wall surface formed with stepped portion". In response to this argument, Examiner would like to point to figure 8 of Hirose '971, which shows the sample chip **2** with a wall surface with stepped portions, after the sample in figure 7. This stepped portion **23** is tungsten film formed through the irradiation of Ga^+ ions in the form of a focus ion beam while a tungsten hexa-carbonyl gas is allowed to flow within the focus ion beam apparatus (see column 4, lines 63 to column 5, line 17). Therefore, Hirose '971 does meet this limitation for claim 1. In addition, Hirose '830 (as cited as prior art for this application) does meet this limitation as a sample chip with two stepped potions are disclosed in Figure 5A .

Applicant further argues that newly submitted independent claims 36, 40, 43, and 47 recite a combination of steps that is not disclosed or suggested by the prior art of record. In response to this argument, Examiner respectfully disagrees, citing that the prior art of record still meets the limitations of the independent claim as well as the dependent claims. See 35 USC 102 and 35 USC103 rejections above for further discussion. No new prior art of record has not been used.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quovaunda Jefferson whose telephone number is 571-272-5051. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

QVJ

MICHELLE ESTRADA
PRIMARY EXAMINER